Course Outcome

The participants are expected to understand:

- Full custom and semi-custom design flow
- Pyxis tool flow for CMOS Design
- Simulation using ELDO simulator
- DC and transient analysis using Pyxis and Ezwave
- Layout Design and Physical verification
- Design rule check and parasitic extraction
- Deep sub-micron condition of MOSFET
- Effects using 60nm and 45nm technology

Assignments and Project

Assignments will be of the following type:

- Lecture sessions
- Instructor led hands-on sessions with 30% lecture and 70% hands on a daily basis
- MCQ model reviews for each topic
- Assignments and Projects

Preferred Pre- Requisites for the Course

The preferred pre-requisites for the course are:

- Basic Electronics.

Hands-on Topics

Lab sessions

- Schematic & HDL code design using Pyxis schematic
- TRAN analysis using Questa ADMS and EZ wave
- Generating physical layout of Common Source amplifier using Pyxis Layout

Registration Fee

Registration Fee
(Including Course Material, Snacks and Lunch)

- **Rs. 1,000/-** for Faculty, Lab Technicians and Project Staff
- **Rs. 1,500/-** for Industry Personnel, Research Scholars and Students.

Mode of Payment: Online Only (RTGS/NEFT)

For Online Transfer

Bank Name: State Bank of India
Account Name: IIT Guwahati R&D E&ICT Academy
Account No.: 36071160089
IFSC Code: SBIN0014262
Bank Name: State Bank of India
Bank Address: IIT Guwahati, GHY- 39.

Topics Covered

Following topics will be covered during session :

- Full custom and semi-custom design flow
- Pyxis tool flow for CMOS Design
- Simulation using ELDO simulator
- DC and transient analysis using Pyxis and Ezwave
- Layout Design Rule with check rule and parasitic extraction
- Deep sub-micron condition of MOSFET and its effects using 60nm and 45nm technology
- Layout versus Schematic with Calibre tool
- Schematic of Circuits using Pyxis
- Generating physical layout of Circuits using Pyxis Layout and performing physical verification using Calibre tool

Objective of the Course

Course Objective is to provide basic knowledge in full custom and semi-custom design flow, tool flow for CMOS design, layout design rule. The programme will focus on practical aspects and include examples which are relevant to the current industry requirements.

Lab sessions will include the following:

- Generating layout from schematic using Pyxis layout tool
- Removing all DRC errors and create GDS II file
- Removing DRC error in layout with the help of Calibre tool
- Creating a schematic of Common Source amplifier and NAND gate using Pyxis Layout

Contact Details

For more details or any queries please contact
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Phone No: +91-3612583009/3182/7086502139
website: http://eict.iitg.ernet.in/

How to Apply

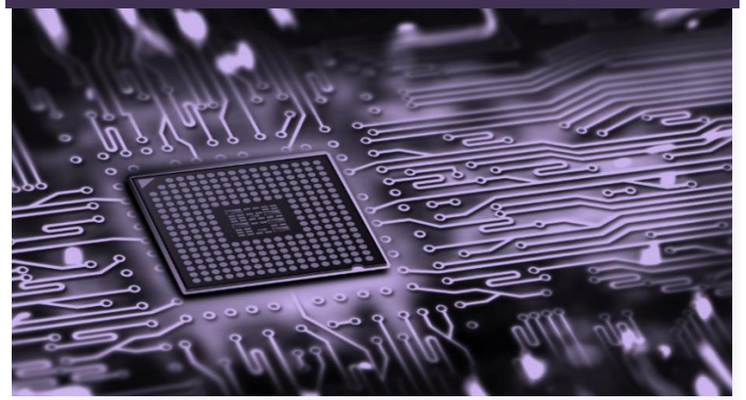
Online Application– The participants may log on to the E&ICT Academy, IIT Guwahati website: http://eictacad@iitg.ernet.in and fill up the google doc application form.

An Initiative of Ministry of Electronics & Information Technology (MeitY), Government of India

Electronics & ICT Academy
IIT Guwahati, Assam

A Three day Workshop on

Mentor Graphics ASIC Design Flow



Organized with support from

CoreEL Technologies

Course Date: 26 – 28 April, 2018
Last Date of Registration: 20.04.2018
(Online Registration Link will be open from 10.03.2018)

Who Can Attend

Programme is open to Faculty Members, Research Scholars, PG & UG Students, Lab Technicians and Project Staffs from Universities , Colleges & Schools. Industry Personnel working in the concerned/allied discipline may also apply.

Contact Hours for the Course
24 Hrs (Theory, Hands-on & Tutorial)