Electronics & ICT Academy

(Under Ministry of Electronics and Information Technology, Government of India)

Indian Institute of Technology Guwahati, Guwahati, Assam, Pin 781039

Phone: +91-361-2582503, 2582536 Email: eictacad@iitg.ernet.in

Venue: Technology complex IIT Guwahati,
Date: 06-08 Oct, 2017

Date	Time	Topic
06-10-2017	9.00am-10.00am	Registration & Reporting
	10.00am-11.30am	• Explain basics of Xilinx seven series FPGA Architecture. • Overview of Xilinx Vivado tool targeting seven series FPGA.
	11.30am-11.45am	Tea Break
	11.45am-01.00pm	• Xilinx Vivado Tool Flow with FPGA based coding techniques • Lab 1: Implement any sequential and combinational design using Xilinx Vivado Tool
	01.00pm-02.00pm	Lunch
	02.00pm-03.00pm	• Synthesis Technique • **Lab 2: Synthesizing a RTL Design** ○ Synthesize a design with the default settings as well as other settings changed and observe the effect.
	03.00pm-04.00pm	• Implementation and Static Timing Analysis • **Lab 3: Implementing the Design** ○ Implement the synthesized design of previous lab, perform timing analysis, generate bitstream, download the bitstream and verify the functionality.
	04.00pm-04.15pm	Tea Break
	04.15pm-05.00pm	Session Continue
07-10-2017	10.00am-11.30am	• IP Integrator • **Lab 4: Using the IP Catalog and IP Integrator** ○ Use the IP Catalog to generate a clock resource and instantiate in a design. Use IP Integrate to generate a core and instantiate in the design.
	11.30am-11.45am	Tea Break
	11.45am-01.00pm	• Xilinx Design Constraints ○ timing analysis.
	01.00pm-02.00pm	Lunch Break
	02.00pm-03.15pm	• **Lab 5: Xilinx Design Constraints**

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		• Create a project with I/O Planning type, enter pin locations, and export it to the rtl. Then create the timing constraints and perform the • Hardware Debugging ○
	03.15pm-04.00pm	• **Lab 6: Hardware Debugging** Use Mark Debug feature and also available Integrated Logic Analyzer(ILA) core (available in IP Catalog) to debug the hardware.
	04.00pm-04.15pm	Tea Break
	04.15pm-05.00pm	Session Continue
08-10-2017	10.00am-11.30am	• Introduction to Embedded System Design using MicroBlaze soft processor • **Lab 7: Simple Hardware Design** ○ Create a Vivado project and use IP Integrator to develop a basic embedded system for a target board.
	11.30am-11.45am	Tea Break
	11.45am-01.00pm	• Zynq Architecture • Extending the Embedded System into Programmable Logic(FPGA)
	01.00pm-02.00pm	Lunch
	02.00pm-03.00pm	**Lab 8: Adding Peripherals in Programmable Logic** • Extend the hardware system by adding AXI peripherals from the IP catalog.
	03.45pm-04.00pm	Tea Break
	04.00pm-05.00pm	**Distribution of Certificates , Feedback, Vote of Thanks**