## Online (LIVE Streaming) Training Programme on “VLSI Chip Design Hands on using Open Source EDA”  
(23 – 27 September, 2019)

<table>
<thead>
<tr>
<th>Module</th>
<th>Lecture</th>
<th>Topics</th>
<th>Tentative Speakers</th>
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</thead>
</table>
| **Module 01**  
*SoC Planning* | Lecture 1 & Lecture 2 | SoC Design :  
- RISC-V and picoSoC overview  
- Overview about SoC planning, like placing pads, macros, memories and IP’s  
- Overview about design cycle, like RTL synthesis, physical design, layout, DRC, clock tree synthesis and STA. | Mr. Kunal P Ghosh  
(Director, VSD Corp. Pvt. Ltd.) |
| **Module 02**  
*Floor planning & timing analysis* | Lecture 3 & Lecture 4 | Pre-layout timing analysis and Floorplanning:  
- Setup/Hold analysis (Theory + Labs)  
- Report nworst, timing_qor, analysis_coverage in clock ideal mode (Theory + Labs)  
- Aspect ratio, utilization factor, power planning (Theory + Labs)  
- Pre-placed cell tap cell, macro, memory/IP placement (Theory + Labs) | Mr. Kunal P Ghosh  
(Director, VSD Corp. Pvt. Ltd.) |
| **Module 03**  
*Placement, Clock tree synthesis* | Lecture 5 & Lecture 6 | Placement, Clock tree synthesis, Routing and SI (Lab – Yosys, Graywolf, Qrouter, OpenSTA, MAGIC)  
- Placement STA with clock ideal (Theory + Labs)  
- CTS quality check – skew, pulse width, duty cycle, latency (Theory + Labs)  
- Routing quality check – signal integrity, delta delay, glitch (Theory + Labs)  
- DRC, LVS check and fix (Theory + Labs) | Mr. Kunal P Ghosh  
(Director, VSD Corp. Pvt. Ltd.) |
| **Module 04**  
*Global routing and Detailed routing* | Lecture 7 & Lecture 8 | Post-layout STA (Lab – OpenSTA)  
- Types of setup/hold checks – reg2reg and IO, clock gating, recovery/removal, data-to-data, latch (time borrow/time given) (Theory + Labs)  
- Need of library, advanced ccs/ecsm concepts, variation (OCV, AOCV, SOCV in brief) | Mr. Kunal P Ghosh  
(Director, VSD Corp. Pvt. Ltd.) |
| **Module 05**  
*LIVE Project* | Lecture 9 & Lecture 10 | SiFive E31 design (Labs)  
- Perform RTL2GDS (including floor planning) of blocks within E31 design  
- Pre-layout and post-layout timing analysis  
- Evaluate block area  
- Integration of all blocks on chip-top  
- Project score analysis | Mr. Kunal P Ghosh  
(Director, VSD Corp. Pvt. Ltd.) |
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**Detailed Schedule of the Programme**

*QnA Timing: - Morning QnA : 11:00 am to 11:15 am  
Afternoon QnA : 01:00 pm to 02:00 pm  
Evening QnA : 04:00 pm to 04:15 pm*

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<tr>
<th>Date/Time</th>
<th>10:00 am to 11:00 am</th>
<th>11:15 am to 01:00 pm</th>
<th>02:00 pm to 04:00 pm</th>
<th>04:15 pm to 05:00 pm</th>
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</table>
| 23-09-2019 Monday | Lecture 1  
Mr. Kunal P Ghosh  
(Director, VSD Corp. Pvt. Ltd.) | Lecture 2  
Mr. Kunal P Ghosh  
(Director, VSD Corp. Pvt. Ltd.) | **Practical Session 01**  
To study the importance of standard cell library and design & characterize one cell using MAGIC Layout tool and ngSPICE for SPICE simulations. | **Practical Session 01 (Continued)** |
| 24-09-2019 Tuesday | Lecture 3  
Mr. Kunal P Ghosh  
(Director, VSD Corp. Pvt. Ltd.) | Lecture 4  
Mr. Kunal P Ghosh  
(Director, VSD Corp. Pvt. Ltd.) | **Practical Session 02**  
To study various components of RISC-V microprocessor based SoC and review all components using MAGIC Layout tool. | **Practical Session 02 (Continued)** |
| 25-09-2019 Wednesday | Lecture 5  
Mr. Kunal P Ghosh  
(Director, VSD Corp. Pvt. Ltd.) | Lecture 6  
Mr. Kunal P Ghosh  
(Director, VSD Corp. Pvt. Ltd.) | **Practical Session 03**  
To do pre-layout timing analysis of SoC using OpenSTA, chip planning using MAGIC and block-level placement/routing using qflow RTL2GDS opensource EDA toolchain. | **Practical Session 03 (Continued)** |
| 26-09-2019 Thursday | Lecture 7  
Mr. Kunal P Ghosh  
(Director, VSD Corp. Pvt. Ltd.) | Lecture 8  
Mr. Kunal P Ghosh  
(Director, VSD Corp. Pvt. Ltd.) | **Practical Session 04**  
To do hierarchical placement/routing using pads and blocks, and perform sign-off checks viz. LVS/DRC using Magic | **Practical Session 04 (Continued)** |
| 27-09-2019 Friday | Lecture 9  
Mr. Kunal P Ghosh  
(Director, VSD Corp. Pvt. Ltd.) | Lecture 10  
Mr. Kunal P Ghosh  
(Director, VSD Corp. Pvt. Ltd.) | **Practical Session 05**  
To perform post-layout timing analysis using OpenSTA and engineering change order (ECO) using Tritonsizer. | Lab Evaluation and Manual Submission |
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<th>Sr. No.</th>
<th>List of Experiments</th>
<th>Sessions</th>
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| 1) | **Aim:** To study the importance of standard cell library and design & characterize one cell using MAGIC Layout tool and ngSPICE for SPICE simulations.  
- System-on-Chip (SoC) planning and design concepts overview  
- Physical design overview  
- Why Libraries are called the soul and heart of semi-conductor industry?  
- Standard cells library overview  
- Art of layout – Stick diagram + Euler’s path using MAGIC  
- Characterization of important parameters using ngSPICE | Practical Session 01 |
| 2) | **Aim:** To study various components of RISC-V microprocessor based SoC and review all components using MAGIC Layout tool.  
- Brief introduction RISC-V ISA  
- Overview of RISC-V based micro-processor and its related SoC  
- Overview of QFN48 package, pads, macros and memory in MAGIC  
- Idea of chip-planning, aspect ratio, utilization factor, power planning, decoupling capacitor, pads/memory and macro placement  
- Pros and cons of good-bad floorplan  
- Introduction to lab to create floorplan for small design, which will be covered in detail on Day 3 | Practical Session 02 |
| 3) | **Aim:** To do pre-layout timing analysis of SoC using OpenSTA, chip planning using MAGIC and block-level placement/routing using qflow RTL2GDS opensource EDA toolchain.  
- Logic synthesis and high fanout net synthesis interactive tutorial using Yosys opensource synthesis tool  
- Introduction to static timing analysis and the related Industry standard reporting formats  
- Pre-layout timing analysis of a design using OpenSTA opensource STA tool, which includes setup timing analysis for reg2reg and IO  
- Introduction to clock tree synthesis (CTS) and its related checks viz. skew, latency, pulse-width, duty cycle  
- Placement/Routing/CTS of a design using qflow opensource RTL2GDS tool  
- Perform CTS quality and routing quality checks using OpenSTA | Practical Session 03 |
| 4) | **Aim:** To do hierarchical placement/routing using pads and blocks, and perform sign-off checks viz. LVS/DRC using Magic  
- Full chip integration using MAGIC for a design with blocks and pads.  
- Revise floorplan from Day 2  
- Populate layout from library manager in MAGIC, select digital core block and additional pads  
- Arrange pads and create a pad-frame hierarchy  
- Abut pads to ensure Padframe is DRC clean  
- Start manual Signal routing and power routing, tie-down unused inputs  
- Add substrate contacts, antenna diodes and pin—labels | Practical Session 04 |
### Practical Session 05

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<th><strong>Aim:</strong> To characterize SiFive E31 design in terms of performance and area using open-source EDA tools</th>
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<tr>
<td></td>
<td>• Review completed layout and perform LVS/DRC checks</td>
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<td>• Perform RTL2GDS (including floor planning) of blocks within E31 design</td>
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### Note:

1. Labs will follow the theory.

**Hardware requirements:** 4GB RAM, 50GB Diskspace, at least 4Mbps internet speed.

3. List of open-source EDA tools used for labs.

<table>
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<tr>
<th>Tools to be installed:</th>
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<tr>
<td>Automated script to install tools</td>
<td><a href="https://github.com/kunalg123/vsdflow">https://github.com/kunalg123/vsdflow</a></td>
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1. ‘vsdflow’ is the TCL engine which installs all necessary open-source EDA tools and its respective dependencies (on ubuntu) needed for workshop. Steps to install are mentioned in the above link.
2. List of tools covered in ‘vsdflow’
   1. Yosys – for Synthesis
   2. Graywolf – for Placement
   3. Qrouter – for Routing
   4. Netgen – for LVS
   5. Magic – for Layout and Floorplanning
   6. Qflow – RTL2GDS integration
   7. OpenSTA & Opentimer – Pre-layout and Post-Layout Static timing analysis
3. There will be some additional PDK’s and scripts needed for workshop, which will be downloaded LIVE.
4. For additional help to install all tools on Windows using Linux virtual box, students can refer to below course