
Jointly organized by: Electronics & ICT Academies at- IIT Guwahati and MNIT Jaipur.

**Course Pre-requisite:** Digital Logic, Hardware Modeling in Verilog/VHDL (basics)

**Hardware Requirement:** Linux Machine with a minimum 2GB RAM (preferably 4GB)

**Tools:** Quartus, Icarus Verilog, EUVM, Gtkwave, Qemu with ARM Ubuntu Image, EUVM

**Note:** Code for all the LABS will be provided on Github

<table>
<thead>
<tr>
<th>Days</th>
<th>Lecture (4 hrs per Day)</th>
<th>Topics</th>
<th>Tentative Speakers</th>
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<tr>
<td>Day 1 (13 July 2020) (06 Hrs)</td>
<td>2 Hrs</td>
<td>• Inauguration: General Introduction: Starts at 9.30AM&lt;br&gt;• Keynote-1 Talk from Mentor-Siemens&lt;br&gt;• Keynote-2 Talk from Intel</td>
<td>1. Mr. Ruchir Dixit, Mentor Graphics&lt;br&gt;2. Mr. Larry Landis, Intel, USA</td>
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<td>2Hrs</td>
<td>• Invited Talk on Emulation by Mentor Graphics</td>
<td>Harish Narayanswamy, Mentor Graphics</td>
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<td>2 Hrs</td>
<td>• SoC design flow, role of Functional Verification and Emulation&lt;br&gt;• Hardware Verification -- Trends and Challenges&lt;br&gt;• Testbench Architecture and Components</td>
<td>Puneet Goel</td>
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<td>Day 2 (14 July 2020) (04 Hrs)</td>
<td>2 Hrs</td>
<td>• Introduction to Intel FPGAs&lt;br&gt;• Overview of Cyclone V FPGA architecture&lt;br&gt;• SoC architecture details &amp; features</td>
<td>Vikas, Intel</td>
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<td></td>
<td>2 Hrs</td>
<td>• Introduction to Quartus &amp; tool flow&lt;br&gt;• LAB: Mapping a simple Design to Cyclone V SoC FPGA</td>
<td>Puneet Goel</td>
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<td>Day 3 (15 July 2020) (04 Hrs)</td>
<td>2 Hrs</td>
<td>• Introduction to UVM, EUVM&lt;br&gt;• Data Types, Structs, Arrays, Queues, and Associative Arrays&lt;br&gt;• Randomization and Constraints -- Constraint Solving -- writing efficient constraint</td>
<td>Puneet Goel</td>
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<td>2 Hrs</td>
<td>• Lab – Simple DuT with native Verilog testbench -- Testbench compilation with Icarus Verilog and Waveform Debug with Gtkwave&lt;br&gt;• Lab – A simple DuT with UVM testbench would be provided – Debug using UVM log reports</td>
<td>Puneet Goel</td>
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<td>Day 4 (16 July 2020) (04 Hrs)</td>
<td>2 Hrs</td>
<td>• Principles of Object-oriented Programming, Classes, Class Interfaces, Inheritance and Polymorphism&lt;br&gt;• Memory Mapped Buses – APB, AHB, Avalon-MM, AXI&lt;br&gt;• Interfacing testbench with DuT -- Bus Functional Models</td>
<td>Puneet Goel</td>
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<td>2 Hrs</td>
<td>• Lab -- Drivers and Monitors in a Testbench -- Writing Bus Functional Models -- Code walk-through for a memory-mapped bus BFM (Driver and Monitor)&lt;br&gt;• Lab – SHA3 DuT with UVM testbench would be provided -- running the testbench and studying the waveforms on the BFM (AXI Bus)</td>
<td>Puneet Goel</td>
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| Day 5 (17 July 2020) (04 Hrs) | 2 Hrs | • Advanced OOP Concepts – Template and Strategy Patterns – UVM testbench architecture  
• UVM Phase and Objection mechanisms | Puneet Goel |
| Day 6 (20 July 2020) (04 Hrs) | 2 Hrs | • Lab – Understanding UVM Sequences and Virtual Sequences | Puneet Goel |
| | 2 Hrs | • Transaction Level Modeling  
• Concepts of TLM Ports, and Connectivity | Puneet Goel |
| | 2 Hrs | • Lab – Code Walkthrough for UVM testbench Connectivity  
• Adding new testcases to the SHA3 testbench | Puneet Goel |
| Day 7 (21 July 2020) (04 Hrs) | 2 Hrs | • Hardware-Software codesign  
• SoC IP Generation – Handoff files  
• Overview SoC-EDS – Eclipse IDE, Device Tree Generator, Linaro Linux* GCC tool chain, ArmCC 5 & ArmCC 6, Debug | Ritesh, Intel |
| | 2 Hrs | LAB: Accessing the FPGA design from C code running on Cyclone V HPS |  |
| Day 8 (22 July 2020) (04 Hrs) | 2 Hrs | • Embedded Linux Concepts – Physical and Virtual Memory  
• Mapping the Testbench to Embedded Linux with DuT on FPGA | Puneet Goel |
| | 2 Hrs | • Simple C code for reading a writing device registers for the DuT mapped on FPGA  
• Lab – Running EUVM testbench for SHA3 DuT on Cyclone V | Puneet Goel |
| | 2 Hrs | • Introduction to Software Emulation using Qemu  
• Hardware-Software Ceverification -- Interfacing a Verilog Simulation with Software stack running on Qemu | Puneet Goel |
| | 2 Hrs | • Lab – Running Qemu based Software Emulation and Coverification with SHA3 DuT Verilog simulation  
(with a EUVM wrapper for simulation interface) | Puneet Goel |
| Day 10 (24 July 2020) (04 Hrs) | 2 Hrs | • Vision Inference using OpenVINO toolkit  
• AI Inferencing on Intel FPGA & use cases  
• Deployment use case | Vikas, Intel |
| Day 9 (23 July 2020) (04 Hrs) | 2 Hrs | • FPGA Hardware Accelerators for HPC workloads  
• Intel FPGA SDK for OpenCL tools usage  
• Development flows for the Acceleration Stack | Ritesh, Intel |
**Speakers Info:**

**Keynote Speakers’ Profile:**

1. **Mr. Ruchir Dixt (Mentor – A Siemens Business):** Ruchir has a strong background in IC design and EDA industry of over the last 20+ years, with various technical, leadership and management roles during the tenure at Mentor Graphics. He has contributed to customer success by working on the complete electronics designs ranging from front-to-back IC design flows (Spec to GDS), PCB design flows. Disciplines have included consulting practice, business development, technical sales and solution design across a broad set of IC design technologies. Ruchir is a natural leader, excellent communicator, results oriented and very driven. He is comfortable operating at executive level to personally motivating a frontline team. He has proven people management and leadership skills, as evidenced by highest employee retention record over a number of years while at the same time executing challenging solutions. Ruchir has Global Leadership Experience having lived in and led teams in USA, and India. Ruchir has worked with customers across different parts of the including USA, Germany, Israel, China, Malaysia and Singapore in true partnerships acting as a trusted advisor to the business. Ruchir has a strong background in IC design and EDA industry of over the last 20+ years, with various technical, leadership and management roles during the tenure at Mentor Graphics. He has contributed to customer success by working on the complete electronics designs ranging from front-to-back IC design flows (Spec to GDS), PCB design flows. Disciplines have included consulting practice, business development, technical sales and solution design across a broad set of IC design technologies. Ruchir is a natural leader, excellent communicator, results oriented and very driven. He is comfortable operating at executive level to personally motivating a frontline team. He has proven people management and leadership skills, as evidenced by highest employee retention record over a number of years while at the same time executing challenging solutions. Ruchir has Global Leadership Experience having lived in and led teams in USA, and India. Ruchir has worked with customers across different parts of the including USA, Germany, Israel, China, Malaysia and Singapore in true partnerships acting as a trusted advisor to the business.

2. **Larry Landis (Senior Manager, University Academic Outreach, Intel Programmable Solutions Group, USA):** Landis has 35 years of experience in a wide variety of functions in the electronics industry including managing the IC development team that designed the first Apple IPOD SoC, marketing, sales and project management for numerous ASIC and FPGA products and most recently running academic outreach for the Intel FPGA division. Mr. Landis teaches part time digital electronics and ASIC design at University of California, Berkeley and Santa Clara University.

**Experts’ Profiles:**

1. **Mr. Puneet Goel:** Puneet has 25 years of experience in the VLSI industry where he worked for STMicro, Motorola, Texas Instruments and TranSwitch. He has two US patents to his credit and was part of the IEEE technical committee that defined the SystemC 1666-2011 standard. He is the lead developer of Embedded UVM.

2. **Vikas Hosoor:** Vikas Hosoor is Field Applications Engineer at Intel’s Programmable Solutions Group. Vikas has been in the VLSI Design Industry for 12+ years and been with Intel for the last 3 years. He has worked as a Design Engineer for 9 years. Working on ASIC and FPGA Designs. At Intel he has been actively involved in helping Customers use Intel FPGAs, Acceleration Stack and OpenVINO. Vikas holds a Master of Engineering from RMIT, Australia and Bachelor of Engineering from Bangalore University.
3. **Ritesh Belgudri**: Ritesh Belgudri is Field Applications Engineer at Intel’s Programable Solutions Group. Prior to joining Intel, he served as a FPGA Architect at Axilware Technologies and various engineering roles at Unizen Technologies. Ritesh is an active IEEE member and author of several International Journal and paper publications. Ritesh holds Bachelor’s in Engineering from University of Mumbai, and Master of Technology in VLSI from Vellore Institute of Technology, Chennai Campus.

4. **Harish Narayanaswamy**: Harish Narayanaswamy is an Application consultant for Emulation at Mentor Graphics a Siemens company. Harish has around 15+ years of EDA industry, has worked on deploying Mentor emulation solutions at ARM, Intel, Qualcomm using Veloce Strato Hardware platform for Verification acceleration. Harish holds Bachelor of Engineering from Bengaluru University.

**Pre-requisite:**

Please find the below pre-requisite online training links.

1. **Basics of Programmable Logic: FPGA Architecture**
2. **Introduction to Verilog HDL**
   https://www.intel.com/content/www/us/en/programmable/support/training/course/ihdl120.html
3. **University Self-Guided Lab: Introduction to FPGAs and the Intel® Quartus® Software**
4. **University Self-Guided Lab: Become an FPGA Designer in 4 Hours**
5. **Introduction to Platform Designer**
6. **Creating a System Design with Platform Designer: Getting Started**
7. **Creating a System Design with Platform Designer: Finish the System**
8. **SoC Hardware Overview: the Microprocessor Unit**
9. **Hardware Design Flow for an Arm*-based Intel® SoC FPGA**
10. **Software Design Flow for an Arm*-based Intel® SoC FPGA**
12. **Introduction to Parallel Computing with OpenCL™ Programs on FPGAs**