Registration

Name of the Applicant (first, last): ……

……

Gender: …….. ……..…

Designation: ……...

Affix passport size photograph

Highest Qualification: ……

Name and Address of the Organization/Institute:……

……..

Category : (GEN/OBC/SC/ST/Others)…….

City/town:……..……..

Email:…….....

Phone Number:……..

Mobile Number:…….....

Do you need accommodation?

(Yes/No):……..

Transaction ID (Applicable for Online Transaction):……

Signature of the Applicant:……...

Signature and Seal of the Forwarding Authority

Name .....

Designation .....

Note: The Faculty/Staff are requested to submit the NOC from respective department before attending the session.. Caste certificate in case of SC/ST/OBC

Registration Fee

Registration Fee (Including Course Material, Snacks and Lunch)

Rs. 2,500/- for Faculty, Lab Technicians and Project Staff **Rs. 5,000/-** for Industry Personnel, Research Scholars and Students.

Mode of Payment: Online Only (RTGS/NEFT)

For Online Transfer

Bank Name: State Bank of India
Account Name: IIT Guwahati R&D E&ICT Academy
Account No.: 36071160089
IFSC Code: SBIN0014262
Bank Name: State Bank of India
Bank Address: IIT Guwahati, GHY- 39.

Course Coordinators

- **Prof. Ratnajit Bhattacharjee**
  Principal Investigator
  E&ICT Academy, IIT Guwahati
- **Prof. Rohit Sinha**
  Co-Principal Investigator
  E&ICT Academy, IIT Guwahati
- **Dr. Gaurav Trivedi**
  Co-Principal Investigator
  E&ICT Academy, IIT Guwahati
- **Dr. Sanjay Kumar Jana**
  Assistant Professor , HOD(I/c)
  ECE Department, NIT Sikkim
- **Mr. Hemant Kumar Kathania**
  Assistant Professor
  ECE Department, NIT Sikkim

Course Coordinator from Industry

- **Mr. Damodara M S**
  Business Head, Entuple Technologies Pvt. Ltd.

Contact Details

For more details or any queries please contact
Program Manager, E&ICT
Academy IIT Guwahati
Email: eictacad@iitg.ernet.in, eictacad@gmail.com
Phone No: +91-3612586442

How To Reach NIT Sikkim

NIT Sikkim is located 2kms away from a town Ravangla Or Ravongla which is a small tourist town situated in South Sikkim district of Sikkim, India. It is connected by a state highway to other major towns in the state and lies between Pelling and Gangtok.You can find your way to the campus using the following link to google maps: goo.gl/kmXGmC
Airways/Railways:
The nearest Airport to reach NIT Sikkim is Bagdogra and nearest railways station is New Jalpaiguri(NJP).
From airport/railway station one has to reach SNT Bus Stand near Siliguri Junction.At the Bus Stand there are various transportation facilities available such as:

सत्यमेव जयते

An Initiative of Department of Electronics & Information Technology (DeitY), Ministry of Communications and IT, Government of India

Electronics & ICT Academy
IIT Guwahati, Assam

A Faculty Development Programme on

Core VLSI Design

Organized in association with NIT Sikkim & Support from

ENTUPLE TECHNOLOGIES

Applications are invited from Faculty Members/ Research Scholars/PG & UG Students/Lab Technicians/Project Staffs from Universities/Colleges/Schools & Industry Personnel working in the concerned discipline can attend the Faculty Development Programme on

"Core VLSI Design "

Course Date: 04-09 April 2017
Last Date of Registration: 1.04.2017
(Online Registration Link will be open from 10.03.2017)
Venue: NIT Sikkim

Course Outcome

The participants are expected to understand:

- Understand FPGA specific coding guidelines in RTL Design
- Compare the RTL for simulation and synthesis in FPGA design flow
- Synthesize the design as per the specification
- Recognize the synthesis and simulation mismatches in RTL Design and its relevance in FPGA design environment
- Use IP cores in FPGA based system design
- Perform timing analysis and interpret timing reports in FPGA based designs
- Illustrate the steps involved in FPGA design implementation
- Work on hardware debugging in FPGA's
- Explain the need for FPGA's in SoC applications

Assignments and Project

Assignments will be of the following type:

- Lecture sessions
- Instructor led hands-on sessions with 30% lecture and 70% hands on a daily basis
- MCQ model reviews for each topic
- Assignments and Projects

Preferred Pre- Requisites for the Course

The preferred pre-requisites for the course are:

- Basic Digital Concepts.
- Basic Knowledge on Verilog.

Hands-on Topics

Lab sessions

- Lab session - Design entry and simulation of given design
- Exercices on STA concepts
- Assignments on modeling of digital blocks

For details of the programme and course contents etc., please log on to Electronics and ICT Academy website: http://eict.iitg.ernet.in/

Topics Covered

Following topics will be covered during session :

- Digital System Design using Verilog.
- Lab session - Design entry and simulation of given design
- Logic Synthesis
- Synthesizable HDL and coding guidelines
- Basics of Timing Analysis
- Exercises on STA concepts
- Interpreting timing reports
- Embedded System Design using FPGA's
- Zynq FPGA architecture & design flow
- Assignments on Modeling of digital blocks.
- Logic Synthesis of the given design using Vivado and results analysis.
- Exercises on STA concepts.

About E&ICT Academy

Electronics and ICT Academy is an initiative of Department of Electronics & Information Technology (DeitY) Ministry of India for Faculty/ Programme. Academy has planned short term training programmes on fundamental and advanced topics in IT, Electronics & Communication, Product Design, Manufacturing with hands on training and project work using latest software tools and systems.
In addition, the Academy will conduct specialized/customized training programmes and research promotion workshops for corporate sector & educational institutions.

About Entuple Technologies Ltd

Entuple Technologies is a next generation solutions enabler in system design technologies across Telecommunication, Defense & Aerospace, Power & Utility segments catering to customer from OEM's, Corporate and Defence and academia

Objective of the Course

Course Objective is to provide basic knowledge in Digital VLSI using FPGA board. The programme will focus on practical aspects and include examples which are relevant to the current industry requirements.
Lab sessions will include the following:

- FPGA design flow using Vivado.
- Digital system design using verilog.
- RTL simulation concepts.
- Implementing Digital Designs on FPGA board using Vivado.
- Clocking resources implementation in Vivado & Static timing analysis.
- Implementing timing analysis using Vivado.
- FSM implementation in Vivado & XSIM simulation
- SOC Designing

Who Can Attend

Programme is open to Faculty Members, Research Scholars, PG & UG Students, Lab Technicians and Project Staffs from Universities , Colleges & Schools. Industry Personnel working in the concerned/allied discipline may also apply.

How to Apply

Online – The participants may log on to the E&ICT Academy, IIT Guwahati website: http://eictacad@iitg.ernet.in and fill up the google doc application form.

Through Email – Scanned copy of the filled in application form duly endorsed by the, forwarding authority is to be mailed at E&ICT Academy's email id (eictacad@gmail.com, eictacad@iitg.ernet.in).

Application format given in this brochure may also be downloaded from the website.

Contact Hours for the Course
48 Hrs (Theory, Hands-on & Tutorial)