CONTACT US

+91-7086502139 (M)
+91-361- 2583182/3199 (O)

eictacad@iitg.ac.in/
eictacad@gmail.com

Website: https://eict.iitg.ac.in/

Address: Project Manager,
E&ICT Academy, IIT Guwahati

IMPORTANT DATES AND TIME

- Start Date of Registration: 12-05-2026
- Last Date of Registration: 01-07-2026
- Per Day Timings: 02.00 pm - 06.00 pm
- Contact Hours: 40 Hrs

(Including Theory, Hands-on & Evaluation)

Registration Fees

Rs. 500/- (Inclusive of GST)

Mode of Payment Online Only
(NEFT/ RTGS /IMPS)

Details for Online Transfer

Bank Name: State Bank of India
Account Name: IIT Guwahati R and D E and ICT Academy
Account No.: 36071160089
IFSC Code: SBIN0014262

SCAN & PAY

UPI ID: eict2025@sbi

ELECTRONICS INDIA
Billion Needs Million Chips

सत्यमेव जयते

Digital India
Power To Empower

An Initiative of Ministry of Electronics & Information Technology (MeitY), Government of India

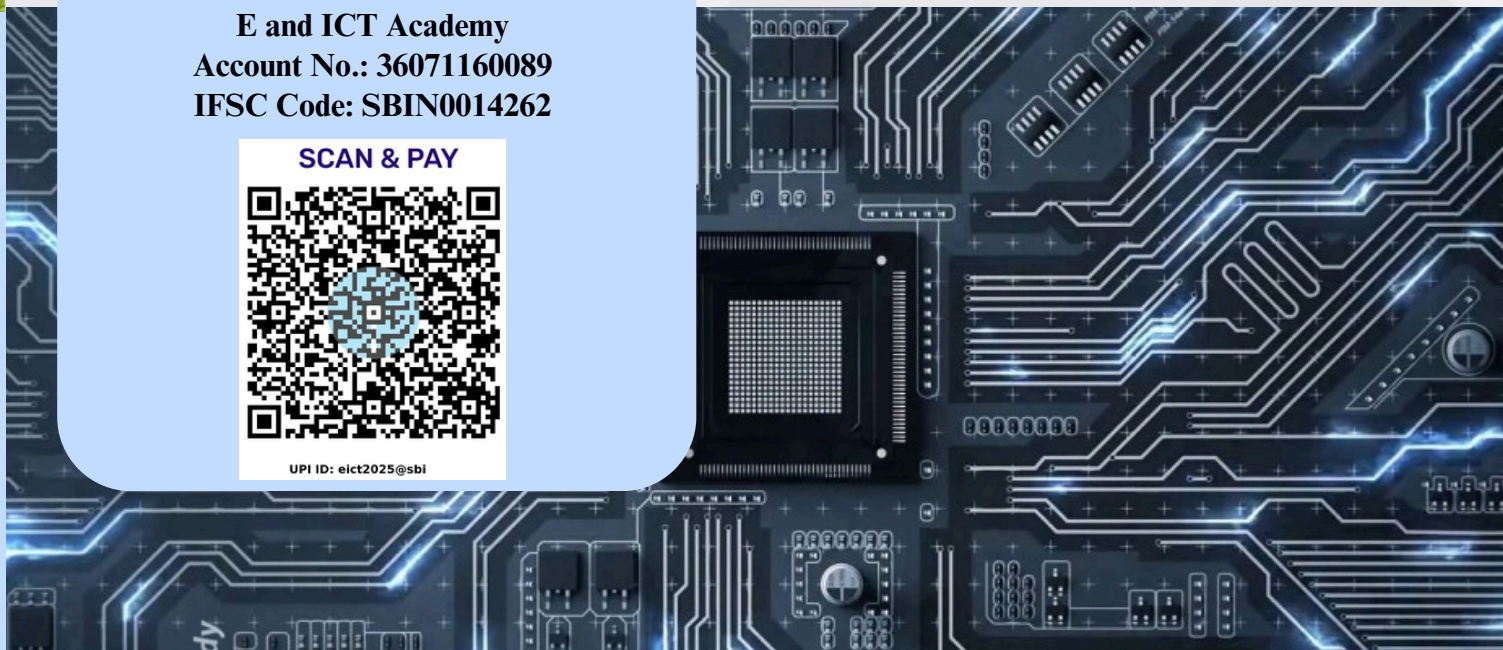
Electronics & ICT Academy
IIT Guwahati, IIT Kanpur, MNIT Jaipur
and IIT Roorkee

Presents

Two - Weeks Joint Faculty Development Programme on

VLSI 102: Digital CMOS Circuit Design

06 July to 17 July 2026



COURSE OBJECTIVES

This two weeks Programme is designed:

1. To introduce participants to the fundamentals of MOS transistor operation and CMOS fabrication technology.
2. To develop understanding of CMOS logic families, inverter characteristics, and digital circuit behavior.
3. To introduce concepts of layout design, design rules, parasitic effects, and physical verification techniques.
4. To train participants in transistor-level circuit design and simulation methodologies using industry-relevant EDA tools.

COURSE OUTCOMES

After successful completion of the course, participants will be able to:

1. Understand the operating principles and characteristics of MOS transistors and CMOS fabrication technology.
2. Analyze and design basic and complex CMOS logic circuits using transistor-level design methodologies.
3. Utilize EDA tools for schematic entry, circuit simulation, verification, and analysis of CMOS circuits.
4. Develop CMOS layouts while adhering to design rules and understand the impact of parasitic effects on circuit performance.
5. Evaluate propagation delay, power dissipation, noise margins, and reliability aspects of CMOS digital circuits.

Principal Coordinators

- **Prof. Gaurav Trivedi**
  IIT Guwahati
  Email ID: trivedi@iitg.ac.in
  Mobile: 0361 2582536
- **Dr. B V Phani**
  IIT Kanpur
  Email: bvphani@eicta.iitk.ac.in
  Mobile: +91 9219972801
- **Dr. Menka Yadav**
  MNIT Jaipur
  Email: menka.ece@mnit.ac.in
  Mobile: 9549650791

ASSIGNMENT AND HANDS-ON

There will be total two MCQ assignments in the entire programme which will be conducted through Google Forms. Hands-on sessions will be followed by the theory lectures.

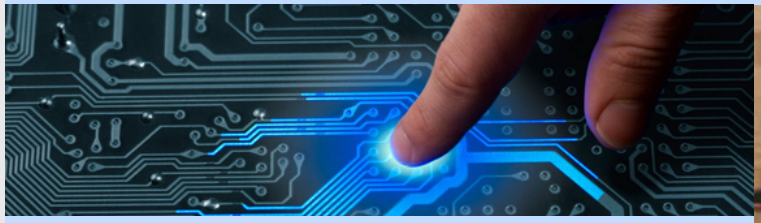
HOW TO REGISTER

Online: The participants may log on to the E&ICT Academy, IIT Guwahati website: **https://eict.iitg.ac.in/index_course_category?cate=em9DWXhJQTVkRkdXMUhQT0dtSjkzQT09**

Registration Link

PLEASE NOTE THESE

- Registration fees includes evaluation and participation certificate.
- Participants have to submit UTR No. as the proof of payment while registering for the Faculty Development Programme.
- Registration Fees is Refundable if the registration cancellation request is submitted before the last date of registration.



Mode of Delivery: Online through Webex