Electronics & ICT Academy

(Under Ministry of Electronics and Information Technology (MeitY), Govt. of India)

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Agenda of Coordinator Sensitization Workshop

Coordinator Sensitization Workshop – on 29th June 2019 – 10am to 12pm IST.

The VSDFLOW utility installation is planned to be covered in this workshop:

1. VSDFLOW is an automated solution to programmers, hobbyists and small-scale semiconductor technology entrepreneurs who can craft their ideas in RTL language, and convert the design to hardware using VSD (RTL-to-GDS) FLOW.
2. VSDFLOW is completely build using OPHW tools, where the user gives input RTL in verilog. From here on the VSDFLOW takes control, RTL is synthesized (using Yosys). The synthesized netlist is given to PNR tool (Qflow) and finally Sign-off is done with STA tool (using Opentimer).
3. The output of the flow is GDSII layout and performance & area metrics of your design.
4. VSDFLOW also provide hooks at all stages for users working at different levels of design flow. It is tested for 30k instance count design like ARM Cortex-M0 and can be further tested for multi-million instance count using hierarchical or glue logic.

Steps to install and run:

- git clone https://github.com/kunalg123/vsdflow.git
- cd vsdflow
- chmod 777 opensource_eda_tool_install.sh
- ./opensource_eda_tool_install.sh
  **NOTE for freshers: This has been tested on a fresh ubuntu installtion
  **NOTE for experienced UNIX users: It has lot of sudo apt-get and sudo remove commands, so you might want to review before running
- ./vsdflow picorv32_design_details.csv

List of Tools installed:

- Yosys - RTL Synthesis
- blifFanout - High fanout net (HFN) synthesis
- graywolf - Placement
- qrouter - Detailed routing
- magic - VLSI Layout tool
- netgen - LVS
- OpenTimer and OpenSTA - Static timing analysis tool