# Electronics & ICT Academy

(Under Ministry of Electronics and Information Technology (MeitY), Govt. of India)

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## *Expert Profile*

Kunal Ghosh is the Director and co-founder of VLSI System Design (VSD) Corp. Pvt. Ltd. Prior to launching VSD in 2017, Kunal held several technical leadership positions at **Qualcomm's Test-chip business unit**. He joined Qualcomm in 2010. **He led the Physical design and STA flow development of 28nm, 16nm test-chips**. At 2013, he joined ***Cadence as Lead Sales Application engineer for Tempus STA tool***. Kunal holds a master's degree in electrical engineering from Indian Institute of Technology (IIT), Bombay, India and specialized in VLSI Design & Nanotechnology.

**Hands on with Technology @**

***1) MSM (mobile station mode chips)*** - MSM chips are used for CDMA modulation/demodulation. It consists of DSP's and microprocessors for running applications such as web-browsing, video conferencing, multimedia services, etc.

***2) Memory test chips*** - Memory test chips are used to validate functionality of 28nm custom/compiler memory as well as characterize their timing, power and yield.

***3) DDR-PHY test chips*** - DDR-PHY test chips are basically tested for high speed data transfer

4) Timing and physical design Flow development for ***130nm MOSFET technology node till 16nm FinFET technology node***.

**5) "*IR aware STA*"** and **"*Low power STA*"**

**6)** Analyzed STA engine behavior for design size up to ***850 million instance count***

***ACADEMIC***

**1)** Research Assistant to Prof. Richard Pinto and Prof. Anil Kottantharayil on "Sub-100nm optimization using Electron Beam Lithography", which intended to optimize RAITH-150TWO Electron Beam Lithography tool and the process conditions to attain minimum resolution, use the mix-and-match capabilities of the tool for ***sub-100nm MOSFET fabrication and generate mask plates for feature sizes above 500nm.***

**2)** Research Assistant to with Prof. Madhav Desai, ***to characterize RTL, generated from C-to-RTL AHIR compiler, in terms of power, performance and area***. This was done by passing RTL, generated from AHIR compiler, through standard ASIC tool chain like synthesis and place & route. The resulting netlist out of PNR was characterized using standard software

***PUBLICATION***

**1)** "**A C-to-RTL Flow as an Energy Efficient Alternative to Embedded Processors in Digital Systems**" submitted in the conference "***13th Euromicro Conference on Digital System Design, Architectures, Methods and Tools, DSD 2010, 1-3 September 2010, Lille, France***"

***2) Concurrent + Distributed MMMC*** STA for 'N' views

**3)** Signoff Timing and Leakage Optimization ***On 18M Instance Count Design With 8000 Clocks*** and Replicated Modules Using Master Clone Methodology With EDI Cockpit

***4) Placement-aware ECO*** Methodology - No Slacking on Slack

**5)** "**Technology mediated tutorial on RISC-V CPU core implementation and sign-off using revolutionary EDA management system (EMS) — VSDFLOW**" published in 2018 China Semiconductor Technology International Conference (CSTIC)