# Electronics & ICT Academy

(Under Ministry of Electronics and Information Technology, Government of India)
Indian Institute of Technology Guwahati, Guwahati, Assam, Pin 781039

Phone: +91-361-253192/3009/+91-7086502139 Email: eictacad@iitg.ac.in

**Venue:** NIT Trichy
**Date:** 30 July- 3 Aug, 2018

| Date | Time | Topic |
|---|---|---|
| 30-07-2018 (Monday) | 09.00am-9.30am | Registration & Reporting |
| | 09.30am-10.00am | Inauguration |
| | 10.00am-11.30am | Introduction<br>Introduction to Xilinx Zynq -7000 SoC |
| | 11.30am-11.45am | Tea Break |
| | 11.45am-01.00pm | • Xilinx Zynq -7000 SoC architecture |
| | 01.00pm-02.00pm | Lunch |
| | 02.00pm-03.00pm | • Xilinx Vivado Tool Flow with Zynq SoC based design techniques<br>**Lab 1: Implement Zynq block design using Xilinx Vivado Tool** |
| | 03.00pm-04.00pm | • Extending embedded design to Artix 7 programmable logic<br>**Lab 2: Adding peripherals in Artix 7 programmable logic along with ARM processing system** |
| | 04.00pm-04.15pm | Tea Break |
| | 04.15pm-07.00pm | • Own Custom IP creation<br>**Lab 3: Adding custom IP with ARM processing system**<br>- Use the Manage IP feature of Vivado to create a custom IP and extend the system with the custom peripheral. |
| 31-07-2018 (Tuesday) | 09.00am-11.30am | • Software Development Environment<br>**Lab 4: Writing Basic Software Applications**<br>• Write a basic C application to access the peripherals. |
| | 11.30am-11.45am | Tea Break |
| | 11.45am-01.00pm | Session Continue |
| | 01.00pm-02.00pm | Lunch Break |
| | 02.00pm-03.15pm | • Software Development and Debugging |
| | 03.15pm-04.00pm | **Lab 5: Software Debugging Using SDK**<br>• Use API to drive CPU's timer. Perform software debugging using SDK |
| | 04.00pm-04.15pm | Tea Break |
| | 04.15pm-06.30pm | • System Debugging using Vivado Logic Analyzer and SDK<br>**Lab 6: Debugging using Vivado Logic Analyzer cores**<br>○ Insert various Vivado Logic Analyzer cores to debug/analyze system behavior. |
| 01-08-2018 (Wednesday) | 09.00am-11.30am | • FPGAs for DSP<br>• Introduction to System Generator for DSP<br>**Lab 7: System Generator design creation** |
| | 11.30am-11.45am | Tea Break |
| | 11.45am-01.00pm | **Lab 8: Design FIR Filter** |
| | 01.00pm-02.00pm | Lunch |
| | 02.00pm-03.45pm | **Lab 9: Grayscale Image enhancement – Image processing** |
| | 03.45pm-04.00pm | Tea |
| | 04.00pm-06.30pm | Vivado HLS and Matlab simulink integration<br>**Lab 10: Median filter design - Hardware co-simulation** |
| | | Vivado static timing analysis<br>Analysing setup time and hold time constraints |

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|---|---|---|
| 02-08-2018 (Thursday) | 09.00am-11.30am | Adding input and output delays<br>**Lab 11: Hardware design using PLL**<br>• Extend the Xilinx 7 series FPGA hardware system by adding PLL with example verilog coding<br>• Synchronous & Asynchronous circuits |
| | 11.30am-11.45am | Tea break |
| | 11.45am-01.00pm | **Lab 12: UART design**<br>• Coding in Verilog and explaining advantages and disadvantages of Xilinx 7 series FPGA clocking resources on the design<br>• Checking/ correcting timing errors |
| | 01.00pm-02.00pm | Lunch |
| | 02.00pm-03.45pm | • Profiling and Performance Improvement<br>• Xilinx Zynq -7000 Cache Coherent Interface and its concepts<br>**Lab 13: Profiling and Performance Tuning**<br>- Profile an application performing a function both in software and hardware. |
| | 03.45pm-04.00pm | Tea break |
| | 04.00pm-06.30pm | **Lab 14: ZYNQ ARM hardcore IP and Microblaze softcore integration**<br>• Extend the hardware system by adding FIFO with example verilog coding |
| 03-08-2018 (Friday) | 09.00am-11.30am | • Introduce the concept of "software-defined" systems on chip (SDSoC)<br>• Get hands-on experience creating application-specific systems on chip from C/C++ programs using the SDSoC tool overview<br>**Lab 15: Getting started with SDSoC design flow**<br>• Go through the process of using SDSoC to create a new project using available templates. |
| | 11.30am-11.45am | Tea Break |
| | 11.45am-01.00pm | • Data motion networks<br>**Lab 16: Pragmas and data motion networks**<br>- Handling data movements between the software and hardware accelerators using various pragmas and SDSoC API. |
| | 01.00pm-02.00pm | Lunch |
| | 02.00pm-03.45pm | • Introduction to CoreEL & Wind River<br>• Wind River Products Portfolio<br>• VxWorks 7 RTOS Detailed Presentation |
| | 03.45pm-04.00pm | Tea break |
| | 04.00pm-05.30pm | • SIMICS Detailed Presentation<br>• VxWorks demonstration in the simulator environment<br>• Q&A Session |
| | 05.30pm-06.30pm | Valedictory Session |