Electronics & ICT Academy

(Under Ministry of Electronics and Information Technology (MeitY), Govt. of India)

Indian Institute of Technology Guwahati, Guwahati, Assam, Pin 781039

Phone: +91-361-2583182/+91 7086502139
Email: eictacad@gmail.com, eictacad@iitg.ac.in

Faculty Development Programme on "VLSI Design at Deep Submicron Node"

Venue: MIT-WPU, Kothrud, Pune.

Date: 18 - 22 February, 2019.

Reporting time on 18th February is 09:00 am.

Date	Time	Topic
18-02-2019 (Day 1)	09.00 am - 09.30 am (30 minutes)	Registration & Reporting
	09.30 am - 10.00 am (30 minutes)	Inauguration
	10.00 am - 10.15 am	Tea Break
	10.15 am - 11.00 am (45 minutes)	Integrated circuit Design - Methodology and EDA Tools
	11.00 am – 12.00 noon (1 Hour)	Digital Design Methodology
	12.00 noon – 01.00 pm (1 Hour)	CMOS Inverter
	01.00 pm - 02.00 pm	Lunch Break
	02.00 pm - 04.00 pm (2 Hours)	Schematic entry using Cadence/Virtuoso
	04.00 pm – 04.15 pm	Tea Break
	04.15 pm – 05.15 pm (1 Hour)	Schematic entry using Cadence/Virtuoso (Continued)
	05.15 pm – 05.30 pm	MCQ - 01
19-02-2019 (Day 2)	09.30 am - 11.00 am (1 Hour 30 minutes)	Coding and Synthesis Guidelines
	11.00 am - 11.15 am	Tea Break
	11.15 am - 01.15 am (2 Hours)	Design of SRAM (stand-alone, embedded, Specs, testing etc)
	01.15 pm - 02.00 pm	Lunch Break
	02.00 pm - 04.00 pm (2 Hours)	Decoder / SRAM bit cell design using cadence
	04.00 pm – 04.15 pm	Tea Break
	04.15 pm – 05.15 pm (1 Hour)	Decoder / SRAM bit cell design using cadence (Continued)
	05.15 pm - 05.30 pm	MCQ - 02
20-02-2019 (Day 3)	09.30 am - 11.00 am (1 Hour 30 minutes)	MOS Analog Models and Application in Circuit design
	11.00 am - 11.15 am	Tea Break
	11.15 am - 01.15pm (2 Hours)	Design of Single T_x Configurations (Controlled Sources)
	01.15 pm - 02.00 pm	Lunch Break

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	02.00 pm - 04.00 pm (2 Hours)	Design of Single Tx AMP using Cadence Tools
	04.00 pm – 04.15 pm	Tea Break
	04.15 pm – 05.15 pm (1 Hour)	Design of Single Tx AMP using Cadence Tools (Continued)
	05.15 pm - 05.30 pm	MCQ - 03
21-02-2019 (Day 4)	09.30 am - 10.30 am (1 Hour)	Analog Simulations (DC, Transient, Noise, Montecarlo, etc)
	10.30 am - 10.45 am	Tea Break
	10.45 am - 11.45 am (1 Hour)	Design of Voltage References/ Sources
	11.45 am – 01.15 pm (1 Hour 30 Minutes)	DRV/LVS/PEX in analog design
	01.15 pm - 02.00 pm	Lunch Break
	02.00 pm - 04.00 pm (2 Hours)	Lab of Voltage Refernce
	04.00 pm – 04.15 pm	Tea Break
	04.15 pm – 05.15 pm (1 Hour)	Lab of Voltage Refernce (Continued)
	05.15 pm - 05.30 pm	MCQ - 04
22-02-2019 (Day 5)	09.30 am - 10.30 am (1 Hour)	Design of Diff AMP / OPAMP
	10.30 am - 10.45 am	Tea Break
	10.45 am - 11.45 am (1 Hour)	Issues in Packaging and testing of VLSI devices
	11.45 am - 12.45 pm (1 Hour)	CMOS Process Fabrication flow
	12.45 pm – 01.15 pm	Issues in Circuit Simulator Design
	01.15 pm - 02.00 pm	Lunch Break
	02.00 pm - 04.00 pm (2 Hours)	Queries on EDA Flow / Tools with Project Assignment
	04.00 pm – 04.15 pm	Tea Break
	04.15 pm - 05:00 pm (1 Hour)	**Open session / Q & A and Feedback**
	05.00 pm - 05.30 pm	Closing Ceremony and Certificate Distribution