Online FDP on Open Power ISA RISC architecture Design (Enabled by Industry IBM) (18-29 Oct, 2021)

Jointly organized by: Electronics & ICT Academies at- IIT Guwahati, NIT Patna, MNIT Jaipur, IIT Roorkee and IIITDM Jabalpur

Day-2-10 (From 10:00 am onwards): Each day lectures will be of 04 Hrs. including 15mins (01 no.) breaks in between.

Date/Time	**9.30 am-10:00 am**	**10.00 am-11:00 am**	**11:00 am-12:00 pm**	**12:00 pm-12:15 pm**	**12:15 pm to 02.00 pm**	
18-10-2020 Monday	**Inauguration and Introduction with all remote centers**	Lightning Talk on Computer Architecture *(Peter Hofstee)*	POWER ISA vs RISC V Comparison *(Vinod)*	**Break (15 mins)**	Microwatt Introduction *(Prof. Satyadhyan)*	
Date/Time	**10:00 am - 12:00 pm**			**12:00 pm-12:15 pm**	**12:15 pm to 02.00 pm**	
19-10-2020 Tuesday	nPOWER ISA *(Prof. Basavaraj Talwar)*			**Break (15 mins)**	FPGA Implementation of Microwatt system *(Manikandan)*	
Date/Time	**10:00 am - 11:00 pm**	**11:00 am - 12:00 pm**		**12:00 pm-12:15 pm**	**12:15 pm to 02.00 pm**	
20-10-2020 Wednesday	System on Chip (SoC) and its Components *(Manikandan)*	Introduction to IP Cores *(Manikandan)*		**Break (15 mins)**	Libre - SoC and its components, tool chains and environment *(Manikandan)*	
Date/Time	**10:00 am - 12:00 pm**			**12:00 pm-12:15 pm**	**12:15 pm to 02.00 pm**	**02.00 pm-02.30 pm**
21-10-2020 Thursday	Impact and use of Wishbone Bus and its protocols *(Manikandan)*			**Break (15 mins)**	Exploring Core to Peripheral and Core to Memory Communication *(Manikandan)*	**Quiz 1**
Date/Time	**10:00 am - 12:00 pm**			**12:00 pm-12:15 pm**	**12:15 pm to 02.00 pm**	
22-10-2019 Friday	Exploring Memory to Memory Communication & Address Space Exploration *(Manikandan)*			**Break (15 mins)**	Porting of design on FPGA and programming *(Manikandan and Varun)*	

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Date/Time	**10:00 am - 11:00 pm**	**11:00 am - 12:00 pm**	**12:00 pm-12:15 pm**	**12:15 pm to 02.00 pm**	
25-10-2020 Monday	Verification concepts – Introduction *(Arjun)*	Verification Open Source Environmental Setup *(Prof. Srinath)*	**Break (15 mins)**	System Verilog Essentials *(Prof. SelvaKumar and Prof. Shashidhara)*	
Date/Time	**10:00 am - 11:00 pm**	**11:00 am - 12:00 pm**	**12:00 pm-12:15 pm**	**12:15 pm to 02.00 pm**	
26-10-2020 Tuesday	Components of IP Core verification *(Prof. SelvaKumar and Prof. Shashidhara)*	Flow of the stimulus in IP verification environment *(Prof. SelvaKumar and Prof. Shashidhara)*	**Break (15 mins)**	Components of SoC verification *(Prof. SelvaKumar and Prof. Shashidhara)*	
Date/Time	**10:00 am - 11:00 pm**	**11:00 am - 12:00 pm**	**12:00 pm-12:15 pm**	**12:15 pm to 02.00 pm**	**02.00 pm-02.30 pm**
27-10-2020 Wednesday	Different testbench automation techniques in IP verification *(Prof. SelvaKumar and Prof. Shashidhara)*	Flow of the stimulus in SoC verification environment *(Prof. SelvaKumar and Prof. Shashidhara)*	**Break (15 mins)**	Describing verification with an example *(Prof. SelvaKumar and Prof. Shashidhara)*	**Quiz 2**
Date/Time	**10:00 am - 12:00 pm**		**12:00 pm-12:15 pm**	**12:15 pm to 02.00 pm**	
28-10-2020 Thursday	Libre-SoC FPGA to ASIC *(Luke Leighton)*		**Break (15 mins)**	Verification Libre-SoC *(Mehul)*	
Date/Time	**10:00 am - 12:00 pm**		**12:00 pm-12:15 pm**	**12:15 pm to 02.00 pm**	**02.00 pm-02.30 pm**
29-10-2019 Friday	OpenLANE Flow for GDS II Generation *(Prof. Srinath)*		**Break (15 mins)**	Coriolos 2 Flow *(Jean-Paul Chaput)*	**Valedictory Session**

*Note: All the lectures and hands-on sessions will be online using Cisco Webex Platform.